IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:	Date: June 21, 2006
Robert T. BAILIS et al.	Confirmation No: 5286
Serial No: 10/016,449	Group Art Unit: 2138
Filed: December 10, 2001	Examiner: John J. Tabone, Jr.

For: METHOD AND SYSTEM FOR USE OF A FIELD PROGRAMMABLE GATE ARRAY (FPGA) FUNCTION WITHIN AN APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC) TO ENABLE CREATION OF A DEBUGGER CLIENT WITHIN THE ASIC

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

REPLY BRIEF ON APPEAL

Pursuant to 37 CFR 1.193(b)(1), Applicant responds to the Examiner's Answer mailed November 16, 2006, as follows:

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the Appeal Brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences is contained in the Appeal Brief.

(3) Status of Claims

A statement identifying the status of the claims is contained in the Appeal Brief.

(4) Status of Amendments

A statement identifying the status of amendments is contained in the Appeal Brief.

(5) Summary of Claimed Subject Matter

A summary of the claimed subject matter is contained in the Appeal Brief.

(6) Grounds of Rejection to be Reviewed on Appeal

A statement identifying the grounds of rejection to be reviewed on appeal is contained in the Appeal Brief.

(7) Response to Examiner's Answer

In the Examiner's Answer on page 9, the Examiner asserts that "indeed the FPGA core 116 performs the functions of monitoring, verifying bug fixes, and detecting errors, not the debugging workstation 104 as the Appellant purports", and the Examiner relies on the Abstract to support such assertion. In particular, the Examiner associates "the programmable portion" (of the Abstract) with the FPGA core 116. Applicant respectfully disagrees with the Examiner's association.

Applicant respectfully submits that "the programmable portion" of the Abstract, instead, refers to the debugging workstation 104 and not the FPGA core 116. The language of the Abstract tracks the language of the paragraph beginning on column 2, line 57, both of which are reproduced below:

> **ABSTRACT** - A system for designing an integrated circuit (IC). The system generally comprising a circuit and a programmable portion used for diagnostics and finding bugs. The circuit generally comprises (i) a functional portion and (ii) a logic portion that may be connected to the functional portion. The logic portion generally includes one or more interfaces. *The programmable*

portion may be configured to detect, correct and/or diagnose errors in the logic portion through the one or more interfaces.

Col. 2, ll. 57-65 - The system 100 generally allows for design of an integrated circuit (IC). The circuit 102 generally comprises a functional portion that varies with design and a logic portion connected to the functional portion (to be discussed in connection with FIGS. 2 and 3). The logic portion generally includes one or more interfaces that may be coupled to the debugging circuit 104. *The debugging circuit 104 may be configured to detect errors in the logic portion through the one or more interfaces.*

Referring to FIG. 1 of Shen, the debugging circuit 104 clearly refers to the debugging workstation 104, which debugging workstation 104 is not contained within the FPGA core 102 (see col. 2, ll. 63-65; FIG. 1). That is, Shen discloses that data is collected from the FPGA core 106 and sent to the debugging workstation where the internal signals are displayed for analysis by a user (e.g., a debugging engineer) (col. 3, ll. 52-57; col. 4, ll. 55-58, col. 5, ll. 13-23).

Accordingly, because Shen discloses performing error detection (and analyzing internal signals) through the debugging workstation 104, Shen, therefore, teaches away from including comparator logic operable to compare selected ones of the plurality of internal signals coupled to the field programmable gate array (FPGA) with a trigger pattern downloaded from the server (as recited in claim 1) within an FPGA. Prior art references must be considered in their entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983). Thus, it would not have been obvious to one of skill in the art that Shen possesses the claimed comparator logic.

Please charge any fee that may be necessary for the continued pendency of this application to Deposit Account No. 09-0460 (IBM Corporation).

Respectfully submitted,
SAWYER LAW GROUP LLP

January 15, 2007
Date

Kelvin M. Vivian
Attorney for Applicant
Reg. No. 53,727
(650) 475-1448

(8) Appendix of Claims

A listing of the claims on appeal is contained in the Appeal Brief.

(9) Evidence Appendix

None.

(10) Related Proceedings Appendix

None.